ABSTRACT

A variable latency elastic buffer comprises a plurality of memory locations in which to hold data. A write and read pointer may point to respective write and read addresses of the plurality of locations in which to write and read data. A controller may hold or increment the address of the read pointer upon determining that the amount of data within the buffer differs from a nominal fill level. In a particular embodiment, initialization circuitry may be operable to initialize the read and write addresses of the respective pointers responsive to an initialization request. The read and write addresses may differ from one another by an offset value equal to a value programmed for the nominal value.